Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 – 12. (cancelled)

13. (new): A liquid crystal display, comprising:

a plurality of data lines;

a plurality of scanning lines and a plurality of conductive lines crossing the plurality of data lines; and

a plurality of pixels positioned at a plurality of matrix-arranged unit areas enclosed by the scanning lines and the data lines, each of the plurality of pixels including a thin film transistor and a liquid crystal capacitor;

wherein a plurality of first conductive lines among the conductive lines is separately modulated relative a plurality of second conductive lines among the conductive lines, and wherein a modulation frequency thereof is synchronized with a scanning frequency of the scanning line.

14. (new): The liquid crystal display of claim 13, wherein the plurality of first conductive lines among the conductive lines are respectively coupled to at least one first transistor, and the plurality of second conductive lines among the conductive lines are respectively coupled to at least one second transistor.

15. (new): The liquid crystal display of Claim 13, further comprising a potential modulation module electrically connected to the first and second conductive lines.

16. (new): The liquid crystal display of Claim 15, wherein the potential modulation module outputs square pulses as potential modulation signals to the first and second conductive lines, and the potential modulation signals respectively applied to two adjacent first and second conductive lines are opposite in phase.

17. (new): The liquid crystal display of Claim 14, wherein each of the first and second transistors has a gate electrode electrically connected to one of the scanning lines, a source electrode electrically connected to the first conductive line or the second conductive line, and a drain electrode electrically connected to a modulation signal source.

18. (new): The liquid crystal display of Claim 17, wherein the drain electrodes of the first transistors are connected to a first modulation signal source, and the drain electrodes of the second transistors are connected to a second modulation signal source.

19. (new): The liquid crystal display of Claim 18, wherein the first modulation signal source and the second modulation signal source separately output square pulses as potential modulation signals opposite in phase .

20. (new): The liquid crystal display of Claim 13, wherein each of the first conductive lines is electrically connected to a first shift register, and each of the second conductive lines is electrically connected to a second shift register.

21. (new): The liquid crystal display of Claim 20, further comprising a modulation signal source electrically connected to one of the first shift registers.

22. (new): The liquid crystal display of Claim 21, wherein the one of the first shift registers shorts to the first conductive line at the first row.

23. (new): The liquid crystal display of Claim 13, wherein the first conductive lines and the second conductive lines are positioned alternatively to each other.

24. (new): The liquid crystal display of Claim 13, wherein the set of the first conductive lines are positioned adjacent to the set of the second conductive lines.

25. (new): The liquid crystal display of Claim 21, wherein an output terminal of the first shift register at the first row is connected to an input terminal of the second shift register next to the first shift register.

26. (new): The liquid crystal display of Claim 22, wherein each of the first and second shift registers has a first potential pin shorting to a first external potential source, a second potential pin shorting to a second external potential source, and a clock pin shorting to the corresponding scanning line.

27. (new): The liquid crystal display of Claim 26, wherein the output terminal of each of the first and second shift registers is at a first potential when the clock pin is selected by the scanning line and while the input terminal of each of the first and second shift registers is at a second potential.